REMARKS

The undersigned wishes to thank the Examiner for the indication that the application is in condition for allowance except for minor informalities. As explained below, the claims have been amended to overcome the minor informalities and explanation has been provided regarding the support for the claims in the specification and drawings. In view the following, Applicants respectfully request that a notice of allowance be issued promptly upon receipt of this amendment.

Claims 1-23, all the claims pending in the application, stand rejected upon informalities. In addition, the drawings are objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. Objections to the Drawings

Figure 10 stands objected to under Rule 84 as not being described fully in the specification. More specifically, the Office Action objects to the reference signs "clk, gate, slower (loaded), gate interest clk output and Cload." Applicants respectfully submit that the elements shown in Figure 10 are abbreviations well known to those ordinarily skilled in the art. More specifically, "clk" is a well-known abbreviation for clock signal; a "gate" is a well-known portion of a transistor; "slower (loaded)" would be understood by one ordinarily skilled in the art to mean that the transistor in question has a load and is slower; the "gate inverse clk output" would readily be understood by one ordinarily skilled in the art to mean that the output is the inverse of the clock seen on the gate; and "Cload" is a well known expression for capacitance load.

Further, Applicants respectfully submit that the forgoing descriptions are so well known by those ordinarily skilled in the art that they do not need to be described fully in the specification. To the contrary, the specification should be limited to a discussion of the novel points of the invention. The specification should not be crowded with detailed discussions of

well-known conventional items so as to avoid making the specification unnecessarily long and to allow the novel aspect of the invention to be quickly and easily understood by the reader. Notwithstanding the foregoing, in order to overcome this rejection, the specification has been amended above, to include brief descriptions of such reference signs. As shown above, since all such reference signs are very well known to those ordinarily skilled in the art and were included with the drawings as originally filed, the forgoing modification to the specification does not introduce new matter but instead merely describes what is clearly shown in the drawings as originally filed.

In addition, the Office Action argues that the features in the claims are not shown in the drawings. Applicants respectfully disagree. For example, with respect to independent claims 1, 11, and 17, the invention is defined as a method for sensing two different types of signals and "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal that an earlier point in time than said second-type of signal is sensed." These features are shown in a number of the drawings included in the application. For example, as shown through Figures 6A and 6B, the invention reduces pessimism by reducing the delay calculation within a circuit by reducing the slew (e.g. utilizing factor K). The delay savings can be seen when comparing Figures 6A and 6B. Figure 6A shows a fairly pessimistic situation wherein the midpoint 601 in the slew of the gate signal 110 must occur substantially before the midpoint 600 in the slew of the clock signal 100. The difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 is shown as time period 605. To the contrary, as shown in Figure 6B, by utilizing a sensing point (e.g., "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal that an earlier point in time than said second-type of signal is sensed" claims 1, 11, and 17) that is well in front of the midpoint 600, 601 (utilizing factor K, assuming no load, etc.), the invention is able to reduce the difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 to a much smaller time 606. In other words, the invention is much less pessimistic and utilizes factor K to observe when the gate

signal just begins its transition. Then, the invention is able to allow this sense point to occur just before when the clock signal begins its transition, as shown in Figure 6B. In doing so, the invention reduces timing delay requirements dramatically.

In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw the objections to the drawings.

II. The 35 U.S.C. 112, First Paragraph, Rejection

The Office Action rejects claims 1-23 under 35 U.S.C. § 112, first paragraph, as not being described in the specification or being seen in the drawings. With respect to independent claims 1, 11, and 17, as argued above, the invention is defined as a method for sensing two different types of signals and "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal that an earlier point in time than said second-type of signal is sensed." These features are shown in a number of the drawings included in the application. For example, as shown through Figures 6A and 6B, the invention reduces pessimism by reducing the delay calculation within a circuit by reducing the slew (e.g. utilizing factor K). The delay savings can be seen when comparing Figures 6A and 6B. Figure 6A shows a fairly pessimistic situation wherein the midpoint 601 in the slew of the gate signal 110 must occur substantially before the midpoint 600 in the slew of the clock signal 100. The difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 is shown as time period 605. To the contrary, as shown in Figure 6B, by utilizing a sensing point (e.g., "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal that an earlier point in time than said second-type of signal is sensed" claims 1, 11, and 17) that is well in front of the midpoint 600, 601 (utilizing factor K, assuming no load, etc.), the invention is able to reduce the difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 to a much smaller time 606. In other words, the invention is much less pessimistic and utilizes factor K to observe when the gate signal just begins its transition. Then, the invention is able to allow this sense point to occur just before when the clock signal begins its

transition, as shown in Figure 6B. In doing so, the invention reduces timing delay requirements dramatically.

With respect to claim 3, Applicants again make reference to Figures 6A and 6B and the discussion of the same in the specification at paragraph 45-48, where it is shown that the input comprises a clock input, and which illustrate clock trailing edge signals. Further, Figure 2 (and the discussion of the same in paragraph 6) discloses that one type of signal causes a transition while in other type of signal prevents a transition.

With respect to claim 8, 15, and 22, the featured of having no load on the output is fully described in paragraph 46. More specifically, the invention relaxes timing rules (decreases pessimism) through a number of mechanisms, such as assuming that there is no load on the gate signal and multiplying the slew by factor K to modify the signal sensing time. The invention realizes that when the logic circuit should block the clock signal, the timing analyzer only needs to observe that the beginning edge of the gate signal transition has started, to find an acceptable timing situation. Thus, the invention recognizes that the logic device (gating device) will stop the clock signal as soon as the gate signal begins to transition to what is logically a blocking (gated) situation. This is also shown in FIG. 8 where the logical AND circuit is shown as item 800 having a clock input 801 which transitions from low to high. These delays and slews 805 may be much longer than they would be for a lightly loaded or unloaded output net 804 attached to the gating device 800 having an output capacitance as shown in FIG. 9.

With respect to claim 9, paragraph 45 explains that, as shown in Figure 6B, by utilizing a sensing point that is well in front of the midpoint 600, 601 (utilizing factor K, assuming no load, etc.), the invention is able to reduce the difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 to a much smaller time 606. In other words, the invention is much less pessimistic and utilizes factor K to observe when the gate signal just begins its transition. Then, the invention is able to allow this sense point to occur just before when the clock signal begins its transition, as shown in Figure 6B. In doing so, the invention reduces timing delay requirements dramatically.

With respect to claim 10, as explained in paragraph 52, the invention uses the least pessimistic of the input-to-input and "propagated" AT tests for the disabling setup test and the enabling hold test. This has much the same effect in situations when the internal dynamics of the gate and the time required for the clock input signal to cause a transition on the output are fast compared to the time required for the gate input signal to cause a transition on the output (i.e., when an asymmetric clock gating circuit is used). The benefit is that it does not require recalculation of the gate delay with zero output load. Further, the Office Action states that the use of the word "conventional" is improper in claims. Applicants respectfully disagree in that some of the features within novel claims can be conventional components. For example, claim 10 defines computing a conventional propagated mode test valued in combination with computing a different value and using the less pessimistic of the two values. This process is novel even though one of the steps within the process may be conventional. Notwithstanding the foregoing, the claim 10 has been amended to remove the term "conventional" in order to speed prosecution.

As shown above, the drawings and specifications fully support and describe the features defined by the claims. Therefore, Applicants respectfully submit that the claims are valid under 35 U.S.C. § 112, first paragraph, and request that this rejection be withdrawn.

III. The 35 U.S.C. 112, Second Paragraph, Rejection

The Office Action rejects claims 7, 14, and 21 as not providing proper antecedent basis for "said gate signal across said gate device." In response, claims 7, 14, and 21 have been amended to define "said gating signals across said gating device" In addition, in claim 7, 14, and 21, "the outputting" has been removed to more clearly define that the modifying prevents "inappropriately reporting a portion of a clock pulse." In view the forgoing, the Examiner is respectfully requested to reconsider and draw these rejections.

In view of the foregoing, Applicants submit that claims 1-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition

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for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 9/23/02

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Marked Up Version Showing Changes Made

[0049] Referring now to FIG. 10, a four-transistor (two p-type T_1, T_2, and two n-type T_3, T_4) gating device 26 is shown as an exemplary NAND clock gating device wherein the second embodiment of the invention as discussed above is implemented using EinsTimer using the methodology taught in U.S. Patent 5,508,937 discussed above. The relative sizes of the transistors is represented by the relative sizes of the transistor symbols T1-T4, showing that T2, which allow the gate signal to force or hold the output high, is smaller than the other transistors. This would cause the $delay_{gate}$ and $Slew_{gate}$ values for the falling gate input and rising gate output to be large, resulting in an unacceptably pessimistic clock gating setup requirement for this gate using the conventional propagated mode clock gating tests. As would be well known to those ordinarily skilled in the art the following reference signs shown in Figure 10 have the following meanings. The reference sign "clk" is an abbreviation for clock signal; a "gate" is a portion of a transistor; "slower (loaded)" means that the transistor in question has a load and is slower; the "gate inverse clk output" means that the output is the inverse of the clock seen on the gate; and "Cload" is an expression for capacitance load.

IN THE CLAIMS:

Please substitute the following claims for the same numbered claims in the application.

7. (Amended) The method in claim 2, wherein said modifying prevents a delay in propagation of said [gate signal] gating signals across said gating device from inappropriately [reporting the] outputting a portion of a clock pulse.

10. (Amended) The method of claim 4, wherein the computing of said setup test comprises:
computing a [conventional] propagated mode test value,
computing an input-to-input test value of zero, and
using the less pessimistic of said computed test values.

14. (Amended) The method in claim 11, wherein said modifying prevents a delay in propagation of said [gate signal] gating signals across said gating device from inappropriately [reporting the] outputting a portion of said clock pulse.

21. (Amended) The program storage device in claim 18, wherein said modifying prevents a delay in propagation of said [gate signal] gating signals across said gating device from inappropriately [reporting the] outputting a portion of a clock pulse.